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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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HAMRE, SCHUMANN, MUELLER & LARSON, P.C.
P.O. BOX 2902-0902
MINNEAPOLIS, MN 55402

| EXAMINER | |
|---|---|
| ZWEIZIG, JEFFERY SHAWN | |
| ART UNIT | PAPER NUMBER |
| 2816 | |

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/726,302 | KURODA, NAOKI | |
| | Examiner | Art Unit | |
| | Jeffrey S. Zweizig | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-5 and 9* is/are allowed.

6)☒ Claim(s) *6* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: Translation

***Withdraw of Allowance***

1. The application has been withdrawn from allowance in light of Applicant's IDS filed 6/21/05.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by JP2001153924.

Fig. 1 discloses a plurality of internal supplies 12/13, a pad 2 and switches P1/P2 that are selectively deactivated as recited in claim 6.

A PTO generated translation is attached to this Office Action.

***Conclusion***

4. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but may be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 2-5 and 9 appear to be allowable over the Prior Art of record. Supplies 12 and 13 do not appear to generate equal

voltages as recited in claim 2. The reference does not appear to disclose shifting circuits as recited in claim 9.

5. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 6/21/05 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

JZ

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-153924

(43)Date of publication of application : 08.06.2001

(51)Int.Cl. G01R 31/28

(21)Application number : 11-338091

(22)Date of filing : 29.11.1999

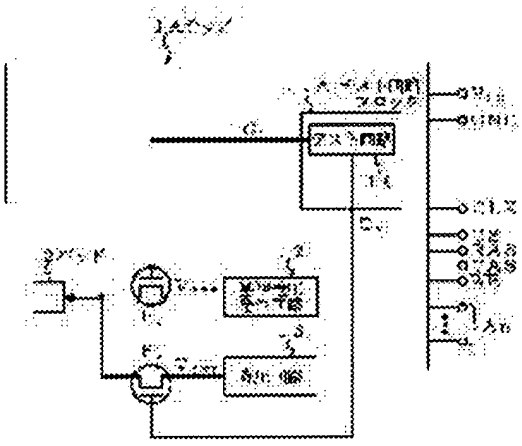
(71)Applicant : NEC IC MICROCOMPUT SYST LTD

(72)Inventor : GOTO KOICHI

## (54) SEMICONDUCTOR STORAGE DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the area of a chip by reducing the number of pads for monitoring and measuring the output voltage of a reference voltage-generating circuit and the output voltage of a step-down circuit in a semiconductor storage device having on the chip at least the step-down circuit, the reference voltage- generating circuit, a test circuit and a plurality of the pads for connecting the chip to the outside.



SOLUTION: The outputs of the reference voltage-generating circuit 12 and the step-down circuit 13 are connected to the same pad 2 via pMOS transistors P1 and P2, respectively. Complementary output signals C1 and C2 from the test circuit 14 are inputted to gate electrodes of the pMOS transistors P1 and P2, thereby complementarily turning the transistors on and off. Accordingly, one pad is shared in place of conventionally required two pads. Since the MOS transistor as a circuit element is small, an area increase by the test circuit 14 and the pMOS transistors P1 and P2 is negligible in comparison with an area decrease by one pad.

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the

examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

## CLAIMS

[Claim(s)]
[Claim 1] The pressure-lowering circuit which lowers the pressure of the supply voltage given from the outside on a chip, and the reference voltage generating circuit which generates the electrical potential difference independent of said supply voltage, The test circuit block for changing a semiconductor memory to test mode according to the signal from the outside, and examining the function of a semiconductor memory, The analog switch which was equipped with two or more pads for electrical installation with the exterior of a chip at least, and was connected each to 1 between the outputting point of said reference voltage generating circuit, and the pad of 1, and between the outputting point of said pressure-lowering circuit, and said pad of 1, It is the means which changes closing motion of said analog switch according to whether the semiconductor memory entered test mode or it does not carry out. The semiconductor memory characterized by having the change means changed so that closing motion of one analog switch and closing motion of the analog switch of another side may keep the complementation mutual.
[Claim 2] The semiconductor memory according to claim 1 characterized by using a metal oxide silicon field effect transistor for said analog switch.
[Claim 3] The semiconductor memory according to claim 2 characterized by said metal oxide silicon field effect transistor being the thing of a p channel mold.
[Claim 4] The semiconductor memory according to claim 2 characterized by said metal oxide silicon field effect transistor being the thing of an n channel mold.
[Claim 5] The semiconductor memory according to claim 4 characterized by changing the flow of said two n channel mold metal oxide silicon field effect transistors, and un-flowing with the complementation by having further the booster circuit which carries out the pressure up of the supply voltage given from the outside, and is supplied on a chip at the gate electrode of the each mold metal oxide silicon field effect transistor of said n channel, and changing the supply place of the output voltage of said booster circuit to the complementation with said change means.
[Claim 6] The pressure-lowering circuit which lowers the pressure of the supply voltage given from the outside on a chip, and the reference voltage generating circuit which generates the electrical potential difference independent of said supply voltage, The test circuit where a condition changes by whether the semiconductor memory entered test mode or it does not carry out and which outputs two signals of the complementation mutually, The 1st p channel mold metal oxide silicon field effect transistor connected so that a current path might be made between two or more pads for electrical installation with the exterior, and the outputting point of said pressure-lowering circuit and one pad in said two or more pads, The 2nd p channel mold metal oxide silicon field effect transistor connected so that a current path might be made between the outputting point of said reference voltage generating circuit and said one pad is included. The semiconductor memory characterized by assigning two output signals of the complementation of said test circuit to every one gate electrode of said 1st and 2nd p channel mold metal oxide silicon field effect transistors, and inputting them.
[Claim 7] The pressure-lowering circuit which lowers the pressure of the supply voltage given from the outside on a chip, and the reference voltage generating circuit which generates the electrical potential difference independent of said supply voltage, The test circuit where a condition changes by whether the semiconductor memory entered test mode or it does not carry out and which outputs two signals of the complementation mutually, The 1st n channel mold metal oxide silicon field effect transistor connected so that a current path might be made between two or more pads for electrical installation with the exterior, and the outputting point of said pressure-lowering circuit and one pad in said

two or more pads, The 2nd n channel mold metal oxide silicon field effect transistor connected so that a current path might be made between the outputting point of said reference voltage generating circuit and said one pad is included. The semiconductor memory characterized by assigning two output signals of the complementation of said test circuit to every one gate electrode of said 1st and 2nd n channel mold metal oxide silicon field effect transistors, and inputting them.

[Claim 8] The pressure-lowering circuit which lowers the pressure of the supply voltage given from the outside on a chip, and the reference voltage generating circuit which generates the electrical potential difference independent of said supply voltage, The test circuit where a condition changes by whether the semiconductor memory entered test mode or it does not carry out and which outputs two signals of the complementation mutually, The circuit which carries out the pressure up of said supply voltage, and two or more pads for electrical installation with the exterior, The 1st n channel mold metal oxide silicon field effect transistor connected so that a current path might be made between the outputting point of said pressure-lowering circuit, and one pad in said two or more pads, The 2nd n channel mold metal oxide silicon field effect transistor connected so that a current path might be made between the outputting point of said reference voltage generating circuit, and said one pad, It is the analog switch connected so that a current path might be made between the outputting point of said booster circuit, and the gate electrode of said 1st n channel mold metal oxide silicon field effect transistor. The analog switch with which closing motion is controlled by one output signal of said test circuit, It is the analog switch connected so that a current path might be made between the outputting point of said booster circuit, and the gate electrode of said 2nd n channel mold metal oxide silicon field effect transistor. The semiconductor memory characterized by equipping closing motion with the analog switch controlled by the output signal of another side of said test circuit.

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[Translation done.]

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to a technique effective in reducing the number of pads on a chip about a semiconductor memory.
[0002]
[Description of the Prior Art] In recent years, large-capacity-izing of a semiconductor memory is remarkable, and, as for the MOS transistor which constitutes the various circuits and memory cell in a chip, flat-surface dimensions, such as gate width and gate length, and three-dimensional dimensions, such as gate oxidation thickness, are made detailed in connection with this. Moreover, dielectric thickness is thin-film-ized in order to secure capacity in spite of contraction of area, even if it is in the capacitor which is one component of a memory cell.
[0003] In the mass storage which constitutes a circuit by the above detailed-izing and the thin-film-ized component For example, destruction and degradation of the gate dielectric film of an MOS transistor and the dielectric film of a capacitor Or in order to prevent aggravation of the transistor characteristics by high electric field being added between the source drains of a short channel MOS transistor etc., as a result to secure the dependability of storage Making lower than the supply voltage (external power electrical potential difference) supplied from the outside of storage supply voltage (internal electrical power source electrical potential difference) which actually operates a circuit within a chip in order to make low the electric field which join a component is performed [ therefore ]. It has the pressure-lowering circuit which lowers an external power electrical potential difference to a predetermined internal electrical power source electrical potential difference. Moreover, when making the pressure lower, in order to obtain the electrical potential difference used as criteria, it has the reference voltage generating circuit for generating the fixed electrical potential difference (reference voltage) independent of an external power electrical potential difference.
[0004] The external power electrical potential difference [ in / to drawing 6 / a semiconductor memory ] VCC, and internal (pressure lowering) supply voltage VINT Reference voltage VREF An example of relation is shown. In drawing 6 , an axis of abscissa expresses the external power electrical potential difference VCC, and an axis of ordinate is each electrical potential difference VCC, VINT, and VREF. It expresses. As shown in drawing 6 , it is reference voltage VREF. While the external power electrical potential difference VCC is low, it is proportional to the external power electrical potential difference VCC, and it is a certain value VCC1 of an external power electrical potential difference. Above, it is concerned with an external power electrical potential difference, and becomes there is nothing and fixed. On the other hand, it is the internal electrical power source electrical potential difference VINT. An external power electrical potential difference is VCC1. It becomes the value same in the following low fields as the external power electrical potential difference VCC, and an external power electrical potential difference is VCC1 -VCC2. In the range, it is reference voltage VREF. The decided constant value is maintained. Furthermore, an external power electrical potential difference is VCC2. In the above field, it becomes a straight line proportional to an external power electrical potential difference. It sets to a semiconductor memory and an external power electrical potential difference is VCC1 -VCC2 to a customer. It is common in the range to guarantee actuation and an external power electrical potential difference is VCC2. The above field is used in the case of the so-called BT (bias tempeh RECHA) trial which applies the temperature and the electrical potential difference more than a coverage of operation to storage in a production process at coincidence, and screens initial failure.
[0005] by the way, output voltage VREF of the reference voltage generating circuit mentioned above Output voltage

VINT of the pressure-lowering circuit as a value and an internal electrical power source electrical potential difference a value -- the margin of a store of operation -- as a result, since a store is the important factor which governs whether it operates normally, it is necessary to grasp those values correctly Then, in order to enable it to measure an electrical potential difference directly from the outside of storage, the outputting point of a reference voltage generating circuit and each pressure-lowering circuit must be pulled out to the pad on a chip (electrode for connection with the exterior of a chip prepared on the chip). In that case, the outputting point of a former and reference voltage generating circuit is each output voltage VREF and VINT, as it connects with the pad of its dedication and the outputting point of a pressure-lowering circuit is also connected to the pad of its dedication on the other hand. Generally outputting to a separate pad is performed. In addition, reference voltage VREF Pressure-lowering supply voltage VINT If the electrical-potential-difference value is that it can measure now from the outside of storage, it is enough and both are not necessarily measured to coincidence.

[0006] An example of a layout of the chip in the above conventional semiconductor memories is typically shown in drawing 7 . With reference to drawing 7 , three circuit blocks, test circuit block 11B, the reference voltage generating circuit 12, and the pressure-lowering circuit 13, are formed in chip 1C shown in this drawing, and two pads 20 and 21 are formed in the border section of a chip. of course -- a chip top -- everything but these three circuits and two pads -- for example, the address decoder of a memory cell array, or a line and a train and a driver -- or Wiring which connects during various kinds of circuit blocks required for storage actuation of **, such as a sense amplifier, and close, an output circuit, and those circuit blocks is formed. Further Although close and an output signal are exchanged between each circuit block and the exterior of a chip or a carrier and many pads for supplying electric power are formed in the external power electrical potential difference VCC, illustration has not been carried out in order to give explanation brief.

[0007] if it is in chip 1C shown in drawing 7 -- the outputting point of the reference voltage generating circuit 12 -- a pad 20 -- linking directly -- the outputting point of the pressure-lowering circuit 13 -- a pad 21 -- linking directly -- **** -- output voltage VREF of a reference voltage generating circuit a pad 20 -- minding -- moreover, output voltage VINT of a pressure-lowering circuit a pad 21 -- minding -- each -- it can measure from the outside.

[0008] It enables it to perform a desired functional test by which test circuit in test circuit block 11B test circuit block 11B activates according to the result of having included some test circuits, having made the store entering test mode when chip select signal CS inputted from the outside, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE were in a certain condition, and having decoded the address signal An at that time. This test circuit block 11B is a circuit usually established in a target at a semiconductor memory, in order to examine the function of storage etc., by the time storage is shipped as a product.

[0009]

[Problem(s) to be Solved by the Invention] As mentioned above, remarkably therefore, an MOS transistor, a component like a capacitor, wiring during a circuit block, etc. are made detailed very much, and large capacity-ization in a semiconductor memory in recent years has the so-called area of internal circuitries, such as a circuit block required for storage actuation, and a memory cell array, in a contraction inclination. However, as for the direction of the pad prepared on a chip, further, it connects with an external connection terminal, for example like a lead terminal prepared in a package by the point, for example, wirebonding etc., and it is in a difficult situation on connection structure with the external connection terminal, or the relation of a method of construction to reduce area from the present condition. Consequently, the area of a chip is greatly influenced increasingly by the number of pads.

[0010] However, the conventional semiconductor memory is the reference voltage VREF without the need of not necessarily measuring both to coincidence. Internal electrical power source electrical potential difference VINT Two pads of dedication are prepared in the sake, respectively. Then, if these two pads can be shared with one pad, the area of a chip can be reduced that much.

[0011] Therefore, this invention is set to the semiconductor memory equipped with two or more pads for connection between a pressure-lowering circuit, a reference voltage generating circuit, a test circuit block, and the exterior of a chip at least on a chip, and aims at reducing the number of pads for supervising and measuring the output voltage of a reference voltage generating circuit, and the output voltage of a pressure-lowering circuit.

[0012]

[Means for Solving the Problem] The pressure-lowering circuit which lowers the pressure of the supply voltage with which the semiconductor memory of this invention is given from the outside on a chip, The reference voltage

generating circuit which generates the electrical potential difference independent of said supply voltage, and the test circuit block for changing a semiconductor memory to test mode according to the signal from the outside, and examining the function of a semiconductor memory, The analog switch which was equipped with two or more pads for electrical installation with the exterior of a chip at least, and was connected each to 1 between the outputting point of said reference voltage generating circuit, and the pad of 1, and between the outputting point of said pressure-lowering circuit, and said pad of 1, It is the means which changes closing motion of said analog switch according to whether the semiconductor memory entered test mode or it does not carry out. It is characterized by having the change means changed so that closing motion of one analog switch and closing motion of the analog switch of another side may keep the complementation mutual.

[0013]

[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained with reference to a drawing. Drawing 1 is drawing showing typically an example of a layout of the chip in the semiconductor memory concerning the gestalt of operation of the 1st of this invention. That compare drawing 1 with drawing 7 and chip 1A concerning the gestalt of this operation differs from chip 1C of the conventional semiconductor memory The number of the pads for amplitude measurements is decreasing to one (pad 2). The output voltage of the reference voltage generating circuit 12 ** The output voltage of the pressure-lowering circuit 13 Between the point and the outputting point of ** reference voltage generating circuit 12 which are outputted through the same pad 2, and a pad 2, p channel mold MOS transistor (pMOS transistor) P1 Between the outputting point of the pressure-lowering circuit 13, and a pad 2, moreover, the pMOS transistor P2 It is that the test circuit 14 for controlling ON of the above-mentioned pMOS transistors P1 and P2 and OFF to the point inserted so that a current path may be made, respectively, and ** test circuit block 11A is extended.

[0014] The signal C1 from a test circuit 14 is inputted into the gate electrode of the pMOS transistor P1, and, on the other hand, similarly, the signal C2 from a test circuit 14 is inputted into the gate electrode of the pMOS transistor P2, respectively. Two signals C1 and C2 are signals of the complementation mutually. A test circuit 14 is an address signal An, when a store enters test mode according to chip select signal CS, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE. Although it is the circuit activated by the signal of the decoded result, both the output signals C1 and C2 are with the time of being in the time of a test circuit 14 being in a non-active state, and an active state, and level interchanges, keeping the relation of the complementation mutual.

[0015] The wave of each signal in the gestalt of this operation of operation is shown in drawing 2 . If chip select signal CS inputted into chip 1A from the exterior at time of day T10, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE change from high level to a low level with reference to drawing 2 , storage will enter test mode in the standup (time of day T11) of the clock signal CLK just behind that, and a test circuit 14 will be activated. Storage is in the usual storage mode of operation before time of day T11, and the test circuit has a non-active state.

[0016] When storage is in the usual storage mode of operation before time of day T11 now, a test circuit 14 is in a non-active state, and is outputting the high-level signal C1 and the signal C2 of a low level. Therefore, it is the internal electrical power source electrical potential difference VINT which the pMOS transistor P1 is turned off, and the pMOS transistor P2 is turned on, and is the output of the pressure-lowering circuit 13 at a pad 2. It is outputted.

[0017] If storage enters test mode at time of day T11, to it and coincidence, the output signal C1 of a test circuit 14 will change from the high level till then to a low level, and a signal C2 will change high-level from a low level. Reference voltage VREF which the pMOS transistor P1 changes from an OFF state to an ON state, and the pMOS transistor P2 changes from an ON state to an OFF state by this, and is the output of the reference voltage generating circuit 12 at a pad 2 It is outputted.

[0018] According to the gestalt of this operation, the output voltage of a reference voltage generating circuit and the output voltage of a pressure-lowering circuit can be changed and measured directly with one pad by making test mode enter and activating a test circuit 14. In that case, chip select signal CS, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE are also an address signal An. Since each is a signal required for the usual storage actuation, a control signal new for the change of the output voltage to a pad 2 is not needed, or a pad does not increase for the input. That is, the one number of pads becomes fewer as the whole storage.

[0019] In the case of the gestalt of this operation, **pMOS transistor of wiring from two (P1, P2), the ** test circuit 14, and the ** test circuit 14 to the gate electrode of the pMOS transistors P1 and P2 increases. Moreover, ** address

signal An It is necessary to add the configuration which chooses a test circuit 14 as a decoder and is made to activate and deactivate. However, since an area required for those reasons is overwhelmingly small compared with the area per pad, with the whole chip, area is reducible by the outline and one pad. For example, as for a pad, in the typical large capacity DRAM, such as 128 etc. megabits, what carried out the about [ 100micrometerx100micrometer ] square per piece is common. On the other hand, typically, for example in an about [ 128M bit ] mass store, the thing whose channel length is 1.0 micrometers and whose channel length is about 0.7 micrometers is used for the MOS transistor which constitutes the internal circuitry in a chip. And a test circuit 14 can constitute about at most eight MOS transistors so that it may mention later, and it is an address signal An. Since some transistors required for the configuration addition of a decoder are also estimated to be extent, the area which increases by the above-mentioned test circuit 14 or the reason of the above-mentioned ** - ** does not become several% of one pad. And since it must arrange regularly on the border of a chip etc. in the case of a pad and the transistor of a test circuit, MOS transistors P1 and P2 as a switch, or wiring can be arranged to the dead space on a chip etc. to the increment in the number of pads influencing a chip area immediately, as long as it goes too far in saying, you may say that there is no effect affect a chip area.

[0020] In addition, in the gestalt of this operation, although the thing of a p channel mold was used for the MOS transistor inserted between the outputting point of the reference voltage generating circuit 12, and a pad 2, and between the outputting point of the pressure-lowering circuit 13, and a pad 2, these transistors can also consist of n channel mold MOS transistors. In that case however, between a pad 2 and the outputting point of the reference potential generating circuit 12, and between a pad 2 and the outputting point of the pressure-lowering circuit 13 The so-called "threshold omission" (in a nMOS transistor) in a nMOS transistor Since the potential difference by the phenomenon which does not become more than the electrical potential difference which deducted the threshold electrical potential difference of a transistor from gate voltage produces a source electrical potential difference when a drain electrical potential difference and gate voltage are given Reference voltage VREF And pressure-lowering supply voltage VINT In order to measure correctly, it is necessary to add the amendment based on the threshold electrical potential difference of a nMOS transistor to the electrical-potential-difference value of the measured pad 2.

[0021] Next, the gestalt of operation of the 2nd of this invention is explained. Drawing 3 is drawing showing typically an example of a layout of the chip in the semiconductor memory concerning the gestalt of operation of the 2nd of this invention. Comparing drawing 3 with drawing 1 and differing from chip 1A which requires chip 1B concerning the gestalt of this operation for the gestalt of the 1st operation ** The point of changing to a pMOS transistor and using the nMOS transistors N1 and N2, ** the gate electrode of these nMOS(s) transistors N1 and N2 -- pressure-up output voltage VB from a booster circuit 15 It is the point of making the complementation turning on and turning off the point of having inputted through the pMOS transistors P3 and P4, respectively, and the ** above-mentioned pMOS transistors P3 and P4, by the signals C1 and C2 from a test circuit 14.

[0022] A booster circuit 15 is a circuit which carries out the pressure up of the external power electrical potential difference VCC to electrical-potential-difference VCC+alpha (=VB) higher than this, for example, it sets to mass DRAM. The signal level which is read from the memory cell of a 1 transistor 1 capacitor configuration to the data line, or is written in a memory cell from the data line In order to prevent falling by the threshold omission in the nMOS transistor as a switch, it is for giving a high electrical potential difference to a word line, and is a circuit indispensable to a mass semiconductor memory conventionally. In the gestalt of this operation, since the booster circuit carried in such a conventional semiconductor memory is diverted as it is, it is not necessary to especially newly form a booster circuit 15, and there is no increment in the chip area by this.

[0023] The wave of each signal in the gestalt of this operation of operation is shown in drawing 4 . With reference to drawing 4 , the usual storage mode-of-operation blank test mode is similarly entered in the gestalt of the 1st operation also in the gestalt of this operation in the standup (time of day T21) of the clock signal CLK immediately after row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE fall from high level to a low level in time of day T20.

[0024] When storage is in the usual storage mode of operation before time of day T21 now, a test circuit 14 is in a non-active state, and is outputting the high-level signal C1 and the signal C2 of a low level. Therefore, the transistor P3 is turned off between two pMOS transistors connected to the outputting point of a test circuit 14. On the other hand, the pMOS transistor P4 is the output voltage VB of a booster circuit 15 to the gate electrode of the nMOS transistor N2 which has been turned on and connected to the pad 2. It is transmitting. Consequently, it is the internal electrical power

source electrical potential difference VINT which a transistor N1 is turned off, and the nMOS transistor N2 is turned on between two nMOS transistors connected to the pad 2, and is the output of the pressure-lowering circuit 13 at a pad 2. It is outputted. Output voltage VB of the booster circuit 15 currently impressed to the gate electrode of the nMOS transistor N2 at this time Since the pressure up is carried out to the electrical potential difference of VCC+alpha higher than supply voltage VCC, there is no threshold omission in the nMOS transistor N2. Therefore, in a pad 2, it is the internal electrical power source electrical potential difference VINT. It is outputted as it is and is the internal electrical power source electrical potential difference VINT. It is not necessary to add amendment to measured value.

[0025] Next, if storage enters test mode at time of day T21, to it and coincidence, the output signal C1 of a test circuit 14 will change from the high level till then to a low level, and a signal C2 will change high-level from a low level. Thereby, between two pMOS transistors connected to the test circuit 14, a transistor P3 changes from an OFF state to an ON state, and changes the pMOS transistor P4 to an OFF state. Consequently, a transistor N1 is the output voltage VB of a booster circuit 15 to a gate electrode between two nMOS transistors connected to the pad 2. It is given and changes from an OFF state to an ON state, and on the other hand, the nMOS transistor N2 changes from an ON state to an OFF state, and the reference voltage VREF which is the output of the reference voltage generating circuit 12 is outputted to a pad 2. Output voltage VB of the booster circuit 15 made into the electrical potential difference of VCC+alpha higher than supply voltage VCC to the gate electrode of the nMOS transistor N1 at this time Since it is impressed, there is no threshold omission in the nMOS transistor N1. Therefore, in a pad 2, it is reference voltage VREF. It is outputted as it is and it is not necessary to add amendment to the measured value.

[0026] The circuit diagram of an example of the test circuit 14 in the gestalt of this operation is shown in drawing 5 . The test circuit 14 shown in this drawing is an address signal An. It activates, when a decoding output is high-level, and when a decoding output is a low level, it is in a non-active state. When a test circuit 14 has a decoding output in a non-active state with a low level now, in the timing chart shown in drawing 4 , in before time of day T21, the nMOS transistors N5 are [ an ON state and N7 ] OFF states, and the pMOS transistor P4 is turned on. Moreover, the nMOS transistor N6 is turned off and, as for the pMOS transistor P3, N8 is turned off by the ON state. Therefore, since the nMOS transistor N2 can give pressure-up electrical-potential-difference VB = VCC+alpha to a gate electrode through the pMOS transistor P4 in drawing 3 , it flows, and it is the output voltage VINT of a pressure-lowering circuit. It outputs to a pad 2. On the other hand, the nMOS transistor N1 intercepts between the outputting point of the reference voltage generating circuit 12, and pads 2.

[0027] On the other hand, when a test circuit 14 has a decoding output in a non-active state with a low level, in the timing chart shown in drawing 4 , the nMOS transistors N5 are [ an OFF state and N7 ] ON states after time-of-day T21, and the pMOS transistor P4 is turned off. Moreover, the nMOS transistor N6 is turned on and, as for the pMOS transistor P3, N8 is turned on by the OFF state. Therefore, in drawing 3 R> 3, the nMOS transistor N1 minds the pMOS transistor P3, and it is the pressure-up electrical potential difference VB to a gate electrode. Since it is given, it flows, and it is the output voltage VREF of a reference voltage generating circuit. It outputs to a pad 2. On the other hand, the nMOS transistor N2 intercepts between the outputting point of the pressure-lowering circuit 13, and pads 2.

[0028] Naturally the test circuit 14 shown in drawing 5 as an example is applicable also to the storage concerning the gestalt of the 1st operation. However, in the gestalt of the 2nd operation, it is different also in the gestalt of the 1st operation, and is the pressure-up electrical potential difference VB. Since it turns on and turns off, it is [ whose gate width is about 3.0 micrometers / whose gate length is about 1.0 micrometers ] more desirable to use a transistor with large size in consideration of high electric field joining the nMOS transistors N5 and N6 in a test circuit 14, rather than it can set in the gestalt of the 1st operation. Moreover, compared with the gestalt of the 1st operation, two pMOS transistors P3 and P4 are required for an excess. Therefore, although those part area becomes large compared with the gestalt of the 1st operation, the increment can be disregarded compared with the area of one pad.

[0029]

[Effect of the Invention] According to this invention, since the pad which was conventionally required for two can be shared with the same pad for the monitor of the output voltage of a reference voltage generating circuit, and the output voltage of a pressure-lowering circuit, and measurement, the part and chip area which decreased in the number of pads are reducible.

[0030] A pMOS transistor or a nMOS transistor can be used for an analog switch. If it constitutes so that the output voltage of the booster circuit usually carried in the conventional store may be inputted into the gate electrode of the nMOS transistor as an analog switch in that case although the amendment of measured value based on the threshold

omission phenomenon of a nMOS transistor is needed when using a nMOS transistor as an analog switch, amendment of measured value will become unnecessary.

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## TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to a technique effective in reducing the number of pads on a chip about a semiconductor memory.

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## PRIOR ART

[Description of the Prior Art] In recent years, large-capacity-izing of a semiconductor memory is remarkable, and, as for the MOS transistor which constitutes the various circuits and memory cell in a chip, flat-surface dimensions, such as gate width and gate length, and three-dimensional dimensions, such as gate oxidation thickness, are made detailed in connection with this. Moreover, dielectric thickness is thin-film-ized in order to secure capacity in spite of contraction of area, even if it is in the capacitor which is one component of a memory cell.
[0003] In the mass storage which constitutes a circuit by the above detailed-izing and the thin-film-ized component For example, destruction and degradation of the gate dielectric film of an MOS transistor and the dielectric film of a capacitor Or in order to prevent aggravation of the transistor characteristics by high electric field being added between the source drains of a short channel MOS transistor etc., as a result to secure the dependability of storage Making lower than the supply voltage (external power electrical potential difference) supplied from the outside of storage supply voltage (internal electrical power source electrical potential difference) which actually operates a circuit within a chip in order to make low the electric field which join a component is performed [ therefore ]. It has the pressure-lowering circuit which lowers an external power electrical potential difference to a predetermined internal electrical power source electrical potential difference. Moreover, when making the pressure lower, in order to obtain the electrical potential difference used as criteria, it has the reference voltage generating circuit for generating the fixed electrical potential difference (reference voltage) independent of an external power electrical potential difference.
[0004] The external power electrical potential difference [ in / to drawing 6 / a semiconductor memory ] VCC, and internal (pressure lowering) supply voltage VINT Reference voltage VREF An example of relation is shown. In drawing 6 , an axis of abscissa expresses the external power electrical potential difference VCC, and an axis of ordinate is each electrical potential difference VCC, VINT, and VREF. It expresses. As shown in drawing 6 , it is reference voltage VREF. While the external power electrical potential difference VCC is low, it is proportional to the external power electrical potential difference VCC, and it is a certain value VCC1 of an external power electrical potential difference. Above, it is concerned with an external power electrical potential difference, and becomes there is nothing and fixed. On the other hand, it is the internal electrical power source electrical potential difference VINT. An external power electrical potential difference is VCC1. It becomes the value same in the following low fields as the external power electrical potential difference VCC, and an external power electrical potential difference is VCC1 -VCC2. In the range, it is reference voltage VREF. The decided constant value is maintained. Furthermore, an external power electrical potential difference is VCC2. In the above field, it becomes a straight line proportional to an external power electrical potential difference. It sets to a semiconductor memory and an external power electrical potential difference is VCC1 -VCC2 to a customer. It is common in the range to guarantee actuation and an external power electrical potential difference is VCC2. The above field is used in the case of the so-called BT (bias tempeh RECHA) trial which applies the temperature and the electrical potential difference more than a coverage of operation to storage in a production process at coincidence, and screens initial failure.
[0005] by the way, output voltage VREF of the reference voltage generating circuit mentioned above Output voltage VINT of the pressure-lowering circuit as a value and an internal electrical power source electrical potential difference a value -- the margin of a store of operation -- as a result, since a store is the important factor which governs whether it operates normally, it is necessary to grasp those values correctly Then, in order to enable it to measure an electrical potential difference directly from the outside of storage, the outputting point of a reference voltage generating circuit and each pressure-lowering circuit must be pulled out to the pad on a chip (electrode for connection with the exterior of

a chip prepared on the chip). In that case, the outputting point of a former and reference voltage generating circuit is each output voltage VREF and VINT, as it connects with the pad of its dedication and the outputting point of a pressure-lowering circuit is also connected to the pad of its dedication on the other hand. Generally outputting to a separate pad is performed. In addition, reference voltage VREF Pressure-lowering supply voltage VINT If the electrical-potential-difference value is that it can measure now from the outside of storage, it is enough and both are not necessarily measured to coincidence.

[0006] An example of a layout of the chip in the above conventional semiconductor memories is typically shown in drawing 7 . With reference to drawing 7 , three circuit blocks, test circuit block 11B, the reference voltage generating circuit 12, and the pressure-lowering circuit 13, are formed in chip 1C shown in this drawing, and two pads 20 and 21 are formed in the border section of a chip. of course -- a chip top -- everything but these three circuits and two pads -- for example, the address decoder of a memory cell array, or a line and a train and a driver -- or Wiring which connects during various kinds of circuit blocks required for storage actuation of **, such as a sense amplifier, and close, an output circuit, and those circuit blocks is formed. Further Although close and an output signal are exchanged between each circuit block and the exterior of a chip or a carrier and many pads for supplying electric power are formed in the external power electrical potential difference VCC, illustration has not been carried out in order to give explanation brief.

[0007] if it is in chip 1C shown in drawing 7 -- the outputting point of the reference voltage generating circuit 12 -- a pad 20 -- linking directly -- the outputting point of the pressure-lowering circuit 13 -- a pad 21 -- linking directly -- **** -- output voltage VREF of a reference voltage generating circuit a pad 20 -- minding -- moreover, output voltage VINT of a pressure-lowering circuit a pad 21 -- minding -- each -- it can measure from the outside.

[0008] It enables it to perform a desired functional test by which test circuit in test circuit block 11B test circuit block 11B activates according to the result of having included some test circuits, having made the store entering test mode when chip select signal CS inputted from the outside, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE were in a certain condition, and having decoded the address signal An at that time. This test circuit block 11B is a circuit usually established in a target at a semiconductor memory, in order to examine the function of storage etc., by the time storage is shipped as a product.

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## EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, since the pad which was conventionally required for two can be shared with the same pad for the monitor of the output voltage of a reference voltage generating circuit, and the output voltage of a pressure-lowering circuit, and measurement, the part and chip area which decreased in the number of pads are reducible.
[0030] A pMOS transistor or a nMOS transistor can be used for an analog switch. If it constitutes so that the output voltage of the booster circuit usually carried in the conventional store may be inputted into the gate electrode of the nMOS transistor as an analog switch in that case although the amendment of measured value based on the threshold omission phenomenon of a nMOS transistor is needed when using a nMOS transistor as an analog switch, amendment of measured value will become unnecessary.

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## TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As mentioned above, remarkably therefore, an MOS transistor, a component like a capacitor, wiring during a circuit block, etc. are made detailed very much, and large capacity-ization in a semiconductor memory in recent years has the so-called area of internal circuitries, such as a circuit block required for storage actuation, and a memory cell array, in a contraction inclination. However, as for the direction of the pad prepared on a chip, further, it connects with an external connection terminal, for example like a lead terminal prepared in a package by the point, for example, wirebonding etc., and it is in a difficult situation on connection structure with the external connection terminal, or the relation of a method of construction to reduce area from the present condition. Consequently, the area of a chip is greatly influenced increasingly by the number of pads.
[0010] However, the conventional semiconductor memory is the reference voltage VREF without the need of not necessarily measuring both to coincidence. Internal electrical power source electrical potential difference VINT Two pads of dedication are prepared in the sake, respectively. Then, if these two pads can be shared with one pad, the area of a chip can be reduced that much.
[0011] Therefore, this invention is set to the semiconductor memory equipped with two or more pads for connection between a pressure-lowering circuit, a reference voltage generating circuit, a test circuit block, and the exterior of a chip at least on a chip, and aims at reducing the number of pads for supervising and measuring the output voltage of a reference voltage generating circuit, and the output voltage of a pressure-lowering circuit.

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MEANS

[Means for Solving the Problem] The pressure-lowering circuit which lowers the pressure of the supply voltage with which the semiconductor memory of this invention is given from the outside on a chip, The reference voltage generating circuit which generates the electrical potential difference independent of said supply voltage, and the test circuit block for changing a semiconductor memory to test mode according to the signal from the outside, and examining the function of a semiconductor memory, The analog switch which was equipped with two or more pads for electrical installation with the exterior of a chip at least, and was connected each to 1 between the outputting point of said reference voltage generating circuit, and the pad of 1, and between the outputting point of said pressure-lowering circuit, and said pad of 1, It is the means which changes closing motion of said analog switch according to whether the semiconductor memory entered test mode or it does not carry out. It is characterized by having the change means changed so that closing motion of one analog switch and closing motion of the analog switch of another side may keep the complementation mutual.
[0013]
[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained with reference to a drawing. Drawing 1 is drawing showing typically an example of a layout of the chip in the semiconductor memory concerning the gestalt of operation of the 1st of this invention. That compare drawing 1 with drawing 7 and chip 1A concerning the gestalt of this operation differs from chip 1C of the conventional semiconductor memory The number of the pads for amplitude measurements is decreasing to one (pad 2). The output voltage of the reference voltage generating circuit 12 ** The output voltage of the pressure-lowering circuit 13 Between the point and the outputting point of ** reference voltage generating circuit 12 which are outputted through the same pad 2, and a pad 2, p channel mold MOS transistor (pMOS transistor) P1 Between the outputting point of the pressure-lowering circuit 13, and a pad 2, moreover, the pMOS transistor P2 It is that the test circuit 14 for controlling ON of the above-mentioned pMOS transistors P1 and P2 and OFF to the point inserted so that a current path may be made, respectively, and ** test circuit block 11A is extended.
[0014] The signal C1 from a test circuit 14 is inputted into the gate electrode of the pMOS transistor P1, and, on the other hand, similarly, the signal C2 from a test circuit 14 is inputted into the gate electrode of the pMOS transistor P2, respectively. Two signals C1 and C2 are signals of the complementation mutually. A test circuit 14 is an address signal An, when a store enters test mode according to chip select signal CS, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE. Although it is the circuit activated by the signal of the decoded result, both the output signals C1 and C2 are with the time of being in the time of a test circuit 14 being in a non-active state, and an active state, and level interchanges, keeping the relation of the complementation mutual.
[0015] The wave of each signal in the gestalt of this operation of operation is shown in drawing 2 . If chip select signal CS inputted into chip 1A from the exterior at time of day T10, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE change from high level to a low level with reference to drawing 2 , storage will enter test mode in the standup (time of day T11) of the clock signal CLK just behind that, and a test circuit 14 will be activated. Storage is in the usual storage mode of operation before time of day T11, and the test circuit has a non-active state.
[0016] When storage is in the usual storage mode of operation before time of day T11 now, a test circuit 14 is in a non-active state, and is outputting the high-level signal C1 and the signal C2 of a low level. Therefore, it is the internal electrical power source electrical potential difference VINT which the pMOS transistor P1 is turned off, and the pMOS

transistor P2 is turned on, and is the output of the pressure-lowering circuit 13 at a pad 2. It is outputted.
[0017] If storage enters test mode at time of day T11, to it and coincidence, the output signal C1 of a test circuit 14 will change from the high level till then to a low level, and a signal C2 will change high-level from a low level. Reference voltage VREF which the pMOS transistor P1 changes from an OFF state to an ON state, and the pMOS transistor P2 changes from an ON state to an OFF state by this, and is the output of the reference voltage generating circuit 12 at a pad 2 It is outputted.
[0018] According to the gestalt of this operation, the output voltage of a reference voltage generating circuit and the output voltage of a pressure-lowering circuit can be changed and measured directly with one pad by making test mode enter and activating a test circuit 14. In that case, chip select signal CS, row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE are also an address signal An. Since each is a signal required for the usual storage actuation, a control signal new for the change of the output voltage to a pad 2 is not needed, or a pad does not increase for the input. That is, the one number of pads becomes fewer as the whole storage.
[0019] In the case of the gestalt of this operation, **pMOS transistor of wiring from two (P1, P2), the ** test circuit 14, and the ** test circuit 14 to the gate electrode of the pMOS transistors P1 and P2 increases. Moreover, ** address signal An It is necessary to add the configuration which chooses a test circuit 14 as a decoder and is made to activate and deactivate. However, since an area required for those reasons is overwhelmingly small compared with the area per pad, with the whole chip, area is reducible by the outline and one pad. For example, as for a pad, in the typical large capacity DRAM, such as 128 etc. megabits, what carried out the about [ 100micrometerx100micrometer ] square per piece is common. On the other hand, typically, for example in an about [ 128M bit ] mass store, the thing whose channel length is 1.0 micrometers and whose channel length is about 0.7 micrometers is used for the MOS transistor which constitutes the internal circuitry in a chip. And a test circuit 14 can constitute about at most eight MOS transistors so that it may mention later, and it is an address signal An. Since some transistors required for the configuration addition of a decoder are also estimated to be extent, the area which increases by the above-mentioned test circuit 14 or the reason of the above-mentioned ** - ** does not become several% of one pad. And since it must arrange regularly on the border of a chip etc. in the case of a pad and the transistor of a test circuit, MOS transistors P1 and P2 as a switch, or wiring can be arranged to the dead space on a chip etc. to the increment in the number of pads influencing a chip area immediately, as long as it goes too far in saying, you may say that there is no effect affect a chip area.
[0020] In addition, in the gestalt of this operation, although the thing of a p channel mold was used for the MOS transistor inserted between the outputting point of the reference voltage generating circuit 12, and a pad 2, and between the outputting point of the pressure-lowering circuit 13, and a pad 2, these transistors can also consist of n channel mold MOS transistors. In that case however, between a pad 2 and the outputting point of the reference potential generating circuit 12, and between a pad 2 and the outputting point of the pressure-lowering circuit 13 The so-called "threshold omission" (in a nMOS transistor) in a nMOS transistor Since the potential difference by the phenomenon which does not become more than the electrical potential difference which deducted the threshold electrical potential difference of a transistor from gate voltage produces a source electrical potential difference when a drain electrical potential difference and gate voltage are given Reference voltage VREF And pressure-lowering supply voltage VINT In order to measure correctly, it is necessary to add the amendment based on the threshold electrical potential difference of a nMOS transistor to the electrical-potential-difference value of the measured pad 2.
[0021] Next, the gestalt of operation of the 2nd of this invention is explained. Drawing 3 is drawing showing typically an example of a layout of the chip in the semiconductor memory concerning the gestalt of operation of the 2nd of this invention. Comparing drawing 3 with drawing 1 and differing from chip 1A which requires chip 1B concerning the gestalt of this operation for the gestalt of the 1st operation ** The point of changing to a pMOS transistor and using the nMOS transistors N1 and N2, ** the gate electrode of these nMOS(s) transistors N1 and N2 -- pressure-up output voltage VB from a booster circuit 15 It is the point of making the complementation turning on and turning off the point of having inputted through the pMOS transistors P3 and P4, respectively, and the ** above-mentioned pMOS transistors P3 and P4, by the signals C1 and C2 from a test circuit 14.
[0022] A booster circuit 15 is a circuit which carries out the pressure up of the external power electrical potential difference VCC to electrical-potential-difference VCC+alpha (=VB) higher than this, for example, it sets to mass DRAM. The signal level which is read from the memory cell of a 1 transistor 1 capacitor configuration to the data line, or is written in a memory cell from the data line In order to prevent falling by the threshold omission in the nMOS

transistor as a switch, it is for giving a high electrical potential difference to a word line, and is a circuit indispensable to a mass semiconductor memory conventionally. In the gestalt of this operation, since the booster circuit carried in such a conventional semiconductor memory is diverted as it is, it is not necessary to especially newly form a booster circuit 15, and there is no increment in the chip area by this.

[0023] The wave of each signal in the gestalt of this operation of operation is shown in drawing 4 . With reference to drawing 4 , the usual storage mode-of-operation blank test mode is similarly entered in the gestalt of the 1st operation also in the gestalt of this operation in the standup (time of day T21) of the clock signal CLK immediately after row address strobe signal RAS, column address strobe signal CAS, and the write enable signal WE fall from high level to a low level in time of day T20.

[0024] When storage is in the usual storage mode of operation before time of day T21 now, a test circuit 14 is in a non-active state, and is outputting the high-level signal C1 and the signal C2 of a low level. Therefore, the transistor P3 is turned off between two pMOS transistors connected to the outputting point of a test circuit 14. On the other hand, the pMOS transistor P4 is the output voltage VB of a booster circuit 15 to the gate electrode of the nMOS transistor N2 which has been turned on and connected to the pad 2. It is transmitting. Consequently, it is the internal electrical power source electrical potential difference VINT which a transistor N1 is turned off, and the nMOS transistor N2 is turned on between two nMOS transistors connected to the pad 2, and is the output of the pressure-lowering circuit 13 at a pad 2. It is outputted. Output voltage VB of the booster circuit 15 currently impressed to the gate electrode of the nMOS transistor N2 at this time Since the pressure up is carried out to the electrical potential difference of VCC+alpha higher than supply voltage VCC, there is no threshold omission in the nMOS transistor N2. Therefore, in a pad 2, it is the internal electrical power source electrical potential difference VINT. It is outputted as it is and is the internal electrical power source electrical potential difference VINT. It is not necessary to add amendment to measured value.

[0025] Next, if storage enters test mode at time of day T21, to it and coincidence, the output signal C1 of a test circuit 14 will change from the high level till then to a low level, and a signal C2 will change high-level from a low level. Thereby, between two pMOS transistors connected to the test circuit 14, a transistor P3 changes from an OFF state to an ON state, and changes the pMOS transistor P4 to an OFF state. Consequently, a transistor N1 is the output voltage VB of a booster circuit 15 to a gate electrode between two nMOS transistors connected to the pad 2. It is given and changes from an OFF state to an ON state, and on the other hand, the nMOS transistor N2 changes from an ON state to an OFF state, and the reference voltage VREF which is the output of the reference voltage generating circuit 12 is outputted to a pad 2. Output voltage VB of the booster circuit 15 made into the electrical potential difference of VCC+alpha higher than supply voltage VCC to the gate electrode of the nMOS transistor N1 at this time Since it is impressed, there is no threshold omission in the nMOS transistor N1. Therefore, in a pad 2, it is reference voltage VREF. It is outputted as it is and it is not necessary to add amendment to the measured value.

[0026] The circuit diagram of an example of the test circuit 14 in the gestalt of this operation is shown in drawing 5 . The test circuit 14 shown in this drawing is an address signal An. It activates, when a decoding output is high-level, and when a decoding output is a low level, it is in a non-active state. When a test circuit 14 has a decoding output in a non-active state with a low level now, in the timing chart shown in drawing 4 , in before time of day T21, the nMOS transistors N5 are [ an ON state and N7 ] OFF states, and the pMOS transistor P4 is turned on. Moreover, the nMOS transistor N6 is turned off and, as for the pMOS transistor P3, N8 is turned off by the ON state. Therefore, since the nMOS transistor N2 can give pressure-up electrical-potential-difference VB = VCC+alpha to a gate electrode through the pMOS transistor P4 in drawing 3 , it flows, and it is the output voltage VINT of a pressure-lowering circuit. It outputs to a pad 2. On the other hand, the nMOS transistor N1 intercepts between the outputting point of the reference voltage generating circuit 12, and pads 2.

[0027] On the other hand, when a test circuit 14 has a decoding output in a non-active state with a low level, in the timing chart shown in drawing 4 , the nMOS transistors N5 are [ an OFF state and N7 ] ON states after time-of-day T21, and the pMOS transistor P4 is turned off. Moreover, the nMOS transistor N6 is turned on and, as for the pMOS transistor P3, N8 is turned on by the OFF state. Therefore, in drawing 3 R> 3, the nMOS transistor N1 minds the pMOS transistor P3, and it is the pressure-up electrical potential difference VB to a gate electrode. Since it is given, it flows, and it is the output voltage VREF of a reference voltage generating circuit. It outputs to a pad 2. On the other hand, the nMOS transistor N2 intercepts between the outputting point of the pressure-lowering circuit 13, and pads 2.

[0028] Naturally the test circuit 14 shown in drawing 5 as an example is applicable also to the storage concerning the gestalt of the 1st operation. However, in the gestalt of the 2nd operation, it is different also in the gestalt of the 1st

operation, and is the pressure-up electrical potential difference VB. Since it turns on and turns off, it is [ whose gate width is about 3.0 micrometers / whose gate length is about 1.0 micrometers ] more desirable to use a transistor with large size in consideration of high electric field joining the nMOS transistors N5 and N6 in a test circuit 14, rather than it can set in the gestalt of the 1st operation. Moreover, compared with the gestalt of the 1st operation, two pMOS transistors P3 and P4 are required for an excess. Therefore, although those part area becomes large compared with the gestalt of the 1st operation, the increment can be disregarded compared with the area of one pad.

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## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing typically an example of the layout of the chip in the semiconductor memory concerning the gestalt of operation of the 1st of this invention.
[Drawing 2] It is drawing showing the wave of each signal in the gestalt of the 1st operation of operation.
[Drawing 3] It is drawing showing typically an example of the layout of the chip in the semiconductor memory concerning the gestalt of operation of the 2nd of this invention.
[Drawing 4] It is drawing showing the wave of each signal in the gestalt of the 2nd operation of operation.
[Drawing 5] It is drawing showing the circuit diagram of an example of a test circuit.
[Drawing 6] It is drawing showing an example of the relation between the external power electrical potential difference in a semiconductor memory, an internal electrical power source electrical potential difference, and reference voltage.
[Drawing 7] It is drawing showing typically an example of the layout of the chip in the semiconductor memory by the Prior art.
[Description of Notations]
1A, 1B, 1C Chip
2 Pad
11A, 11B Test circuit block
12 Reference Voltage Generating Circuit
13 Pressure-Lowering Circuit
14 Test Circuit
15 Booster Circuit
20 21 Pad

[Translation done.]

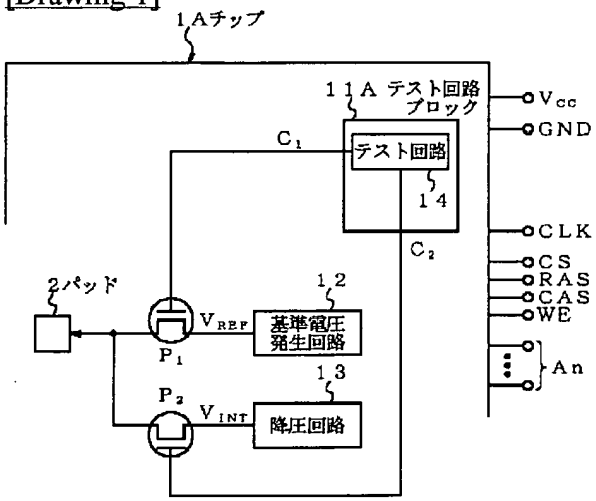
* NOTICES *



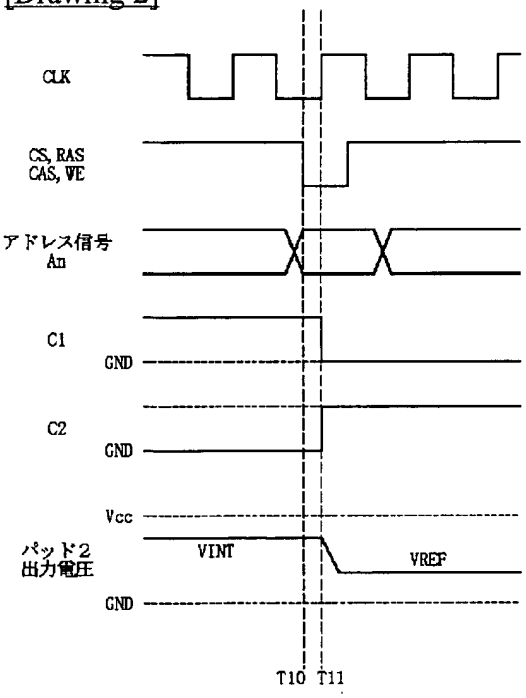
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

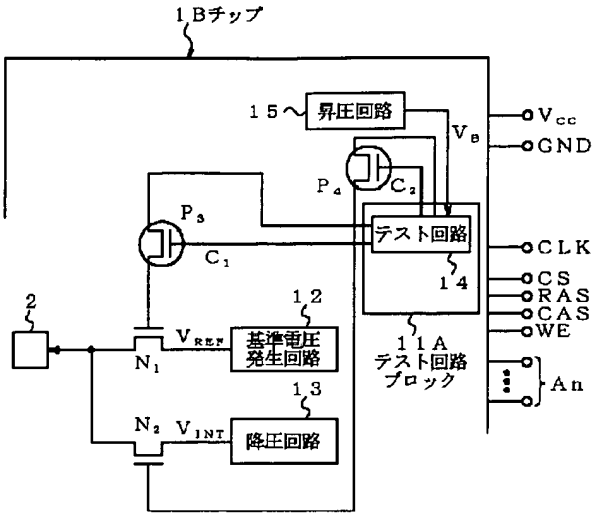
[Drawing 1]



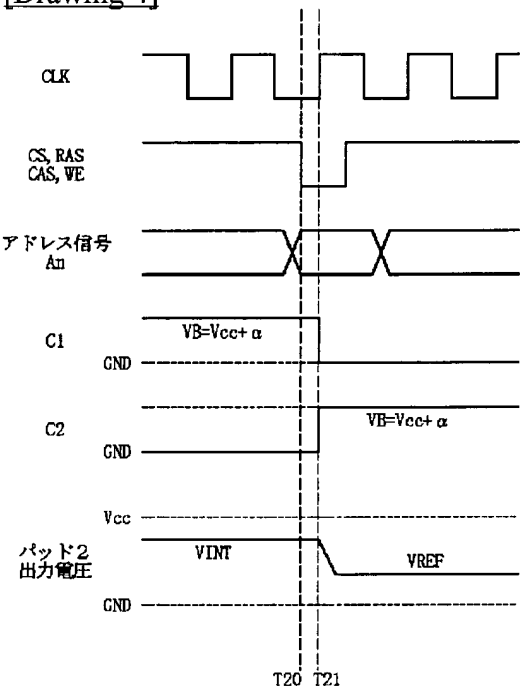

[Drawing 2]



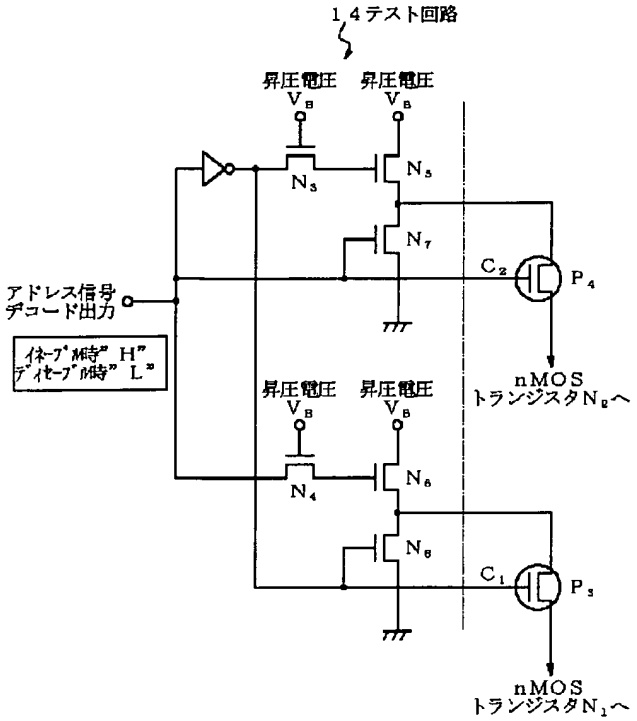

[Drawing 3]



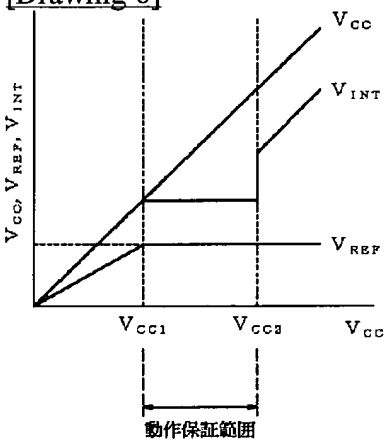

[Drawing 4]



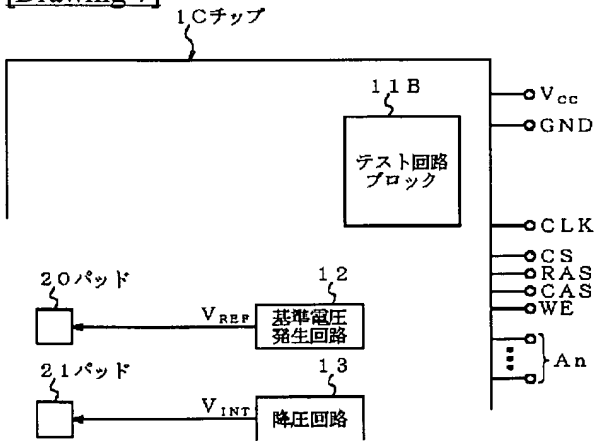

[Drawing 5]




[Drawing 6]




[Drawing 7]



[Translation done.]